

FIG. 1A  
(Prior Art)

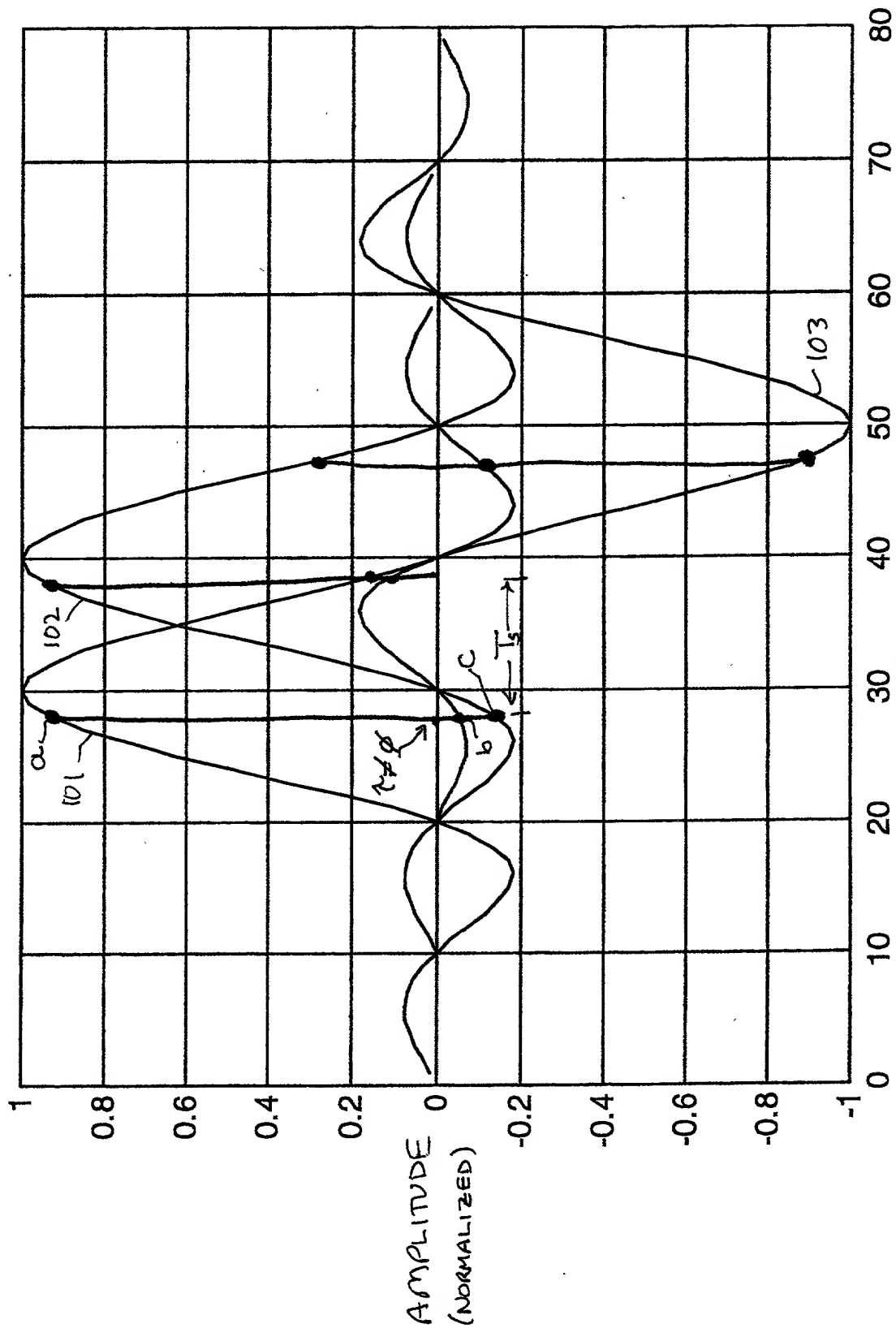


FIG. 1B  
(PRIOR ART)

Non ideal sampling yielding ISI.  $\tau \neq 0$

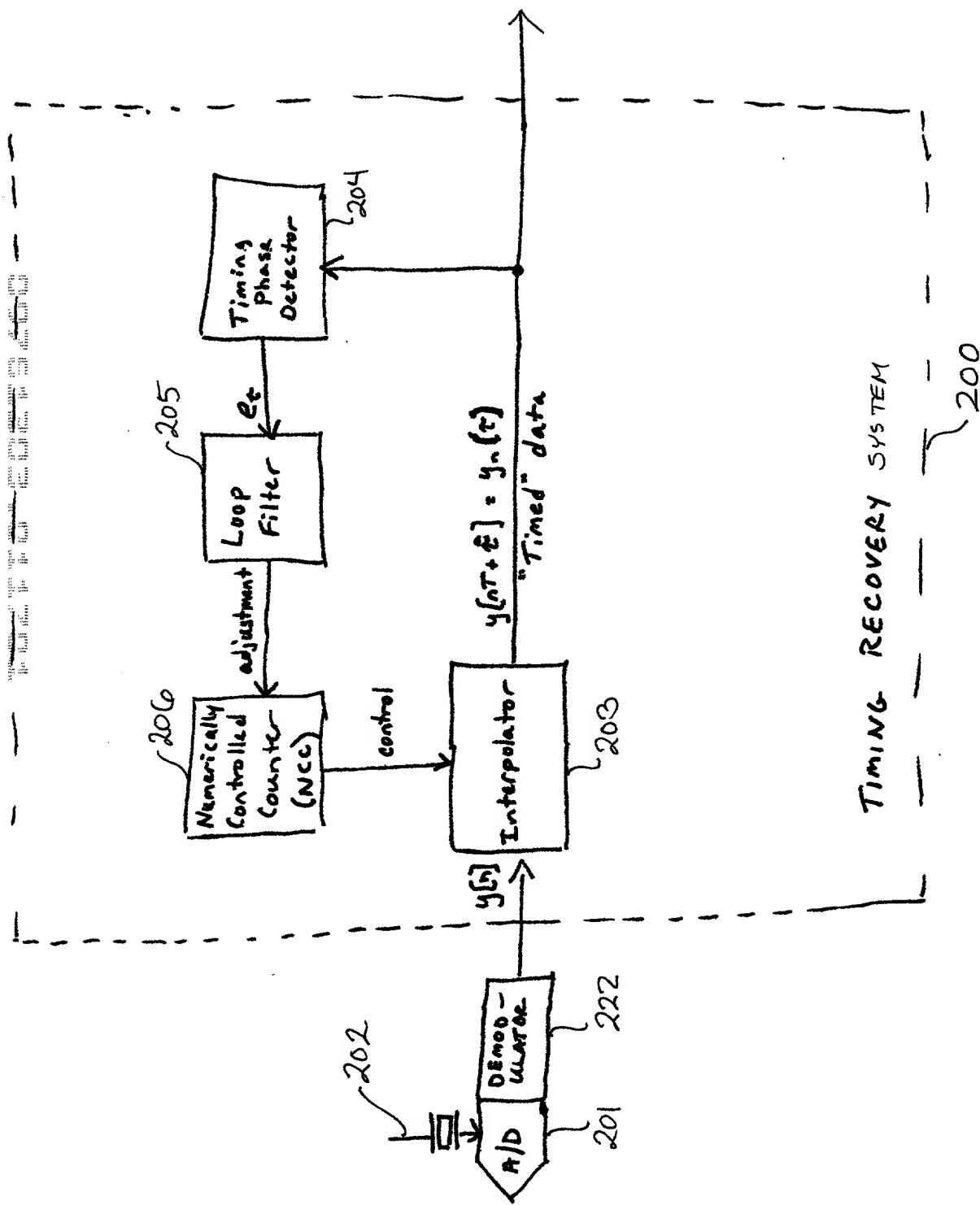


FIG. 2 (Prior Art)

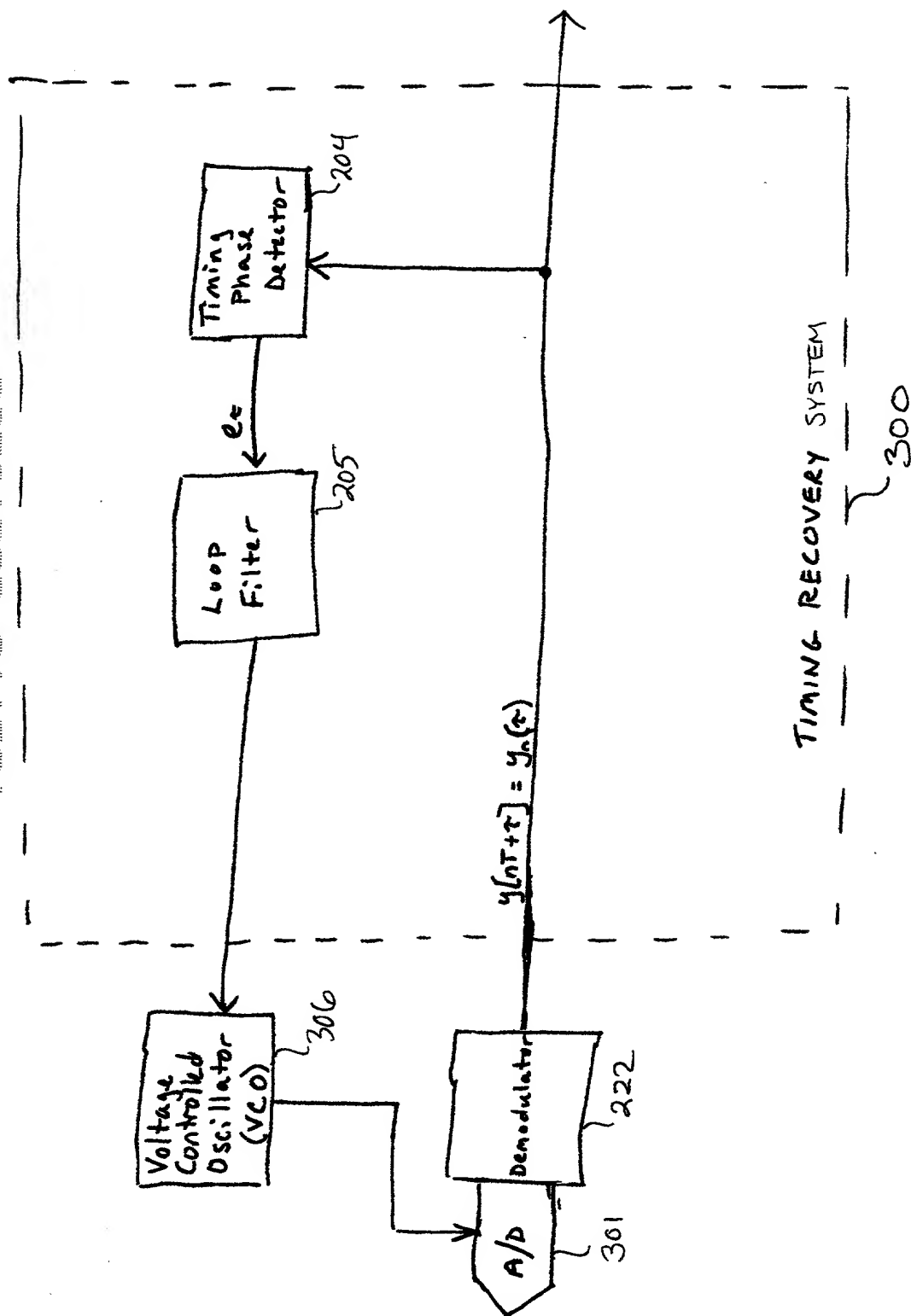
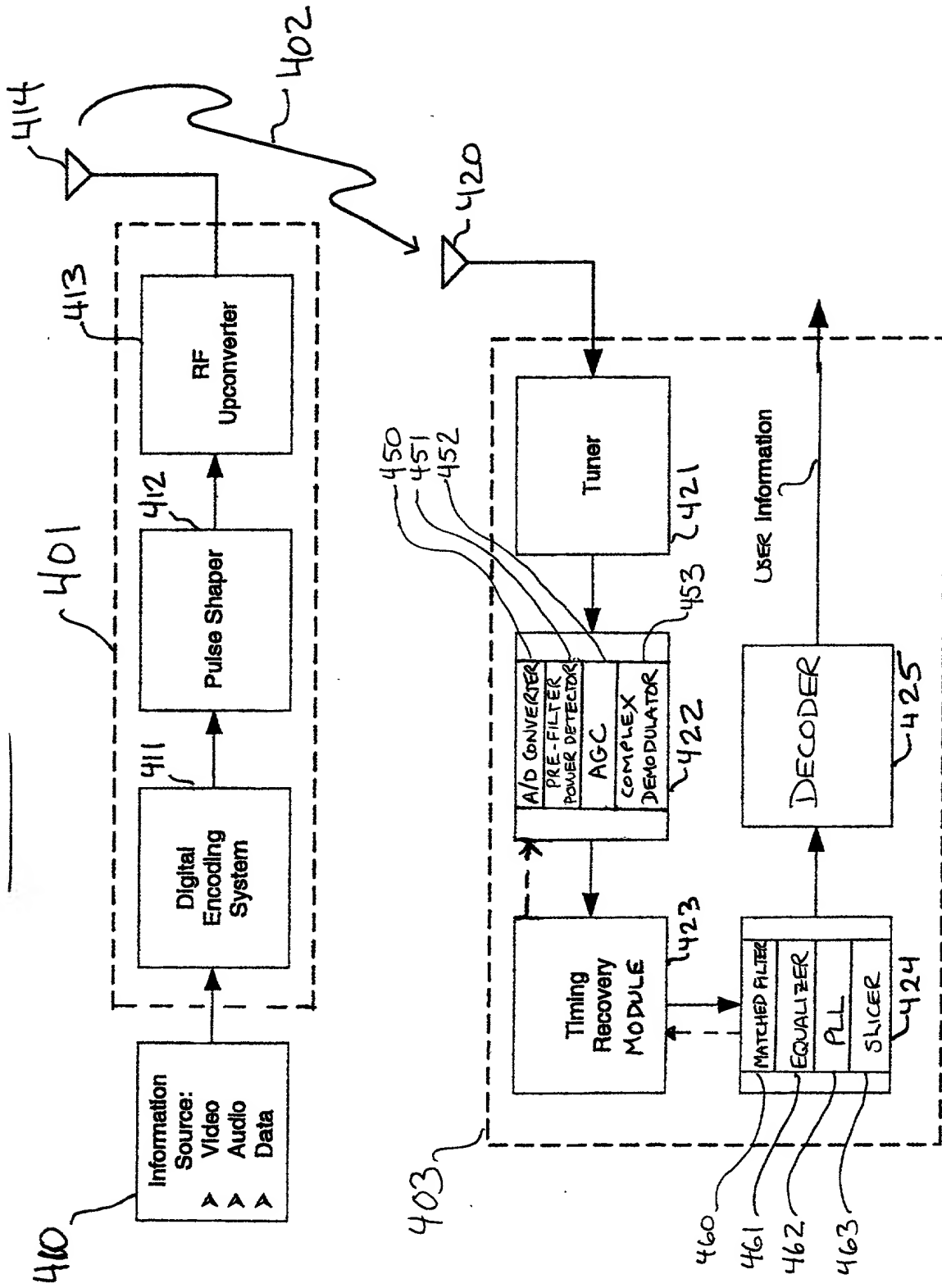


FIG. 3  
(PRIOR ART)

FIG. 4

400



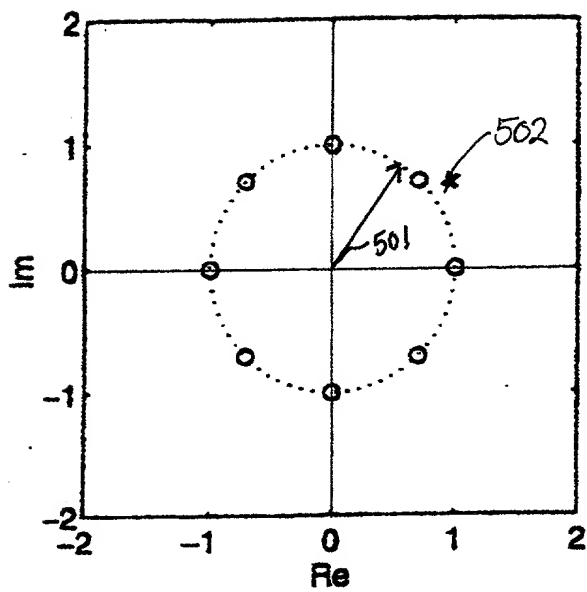


FIG. 5A

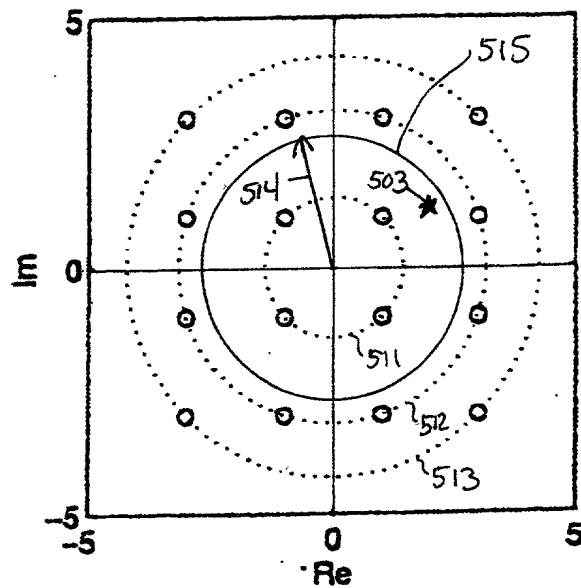


FIG. 5B

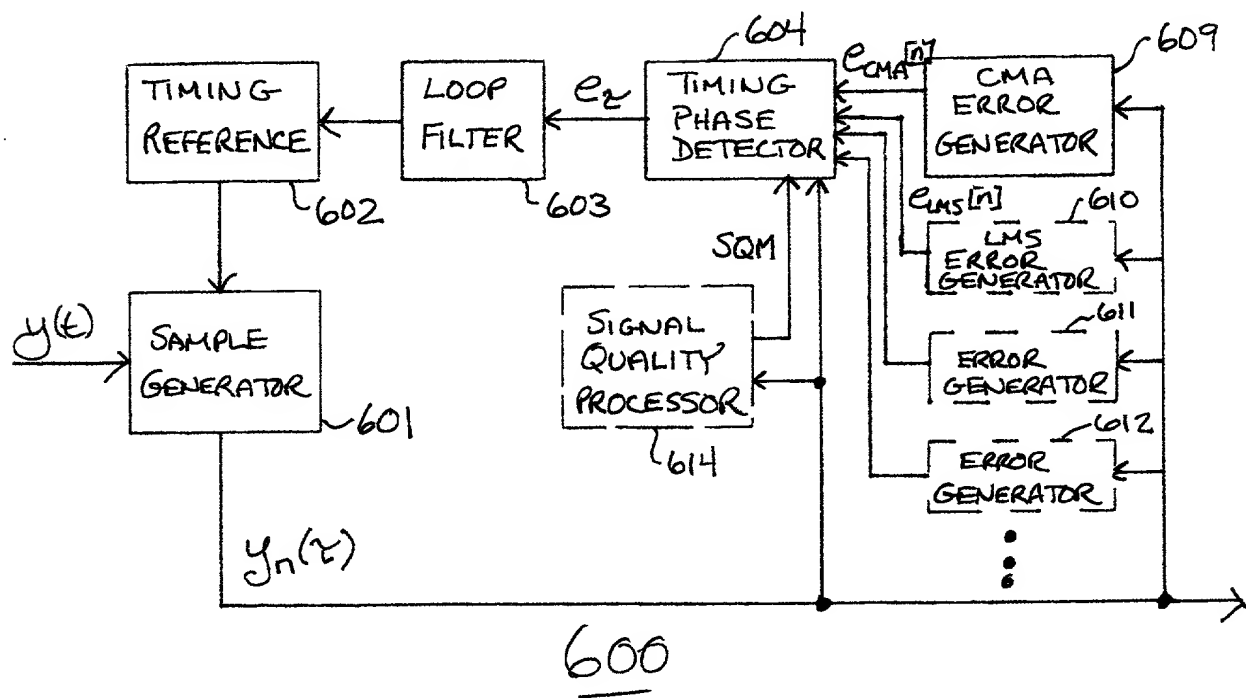


FIG. 6

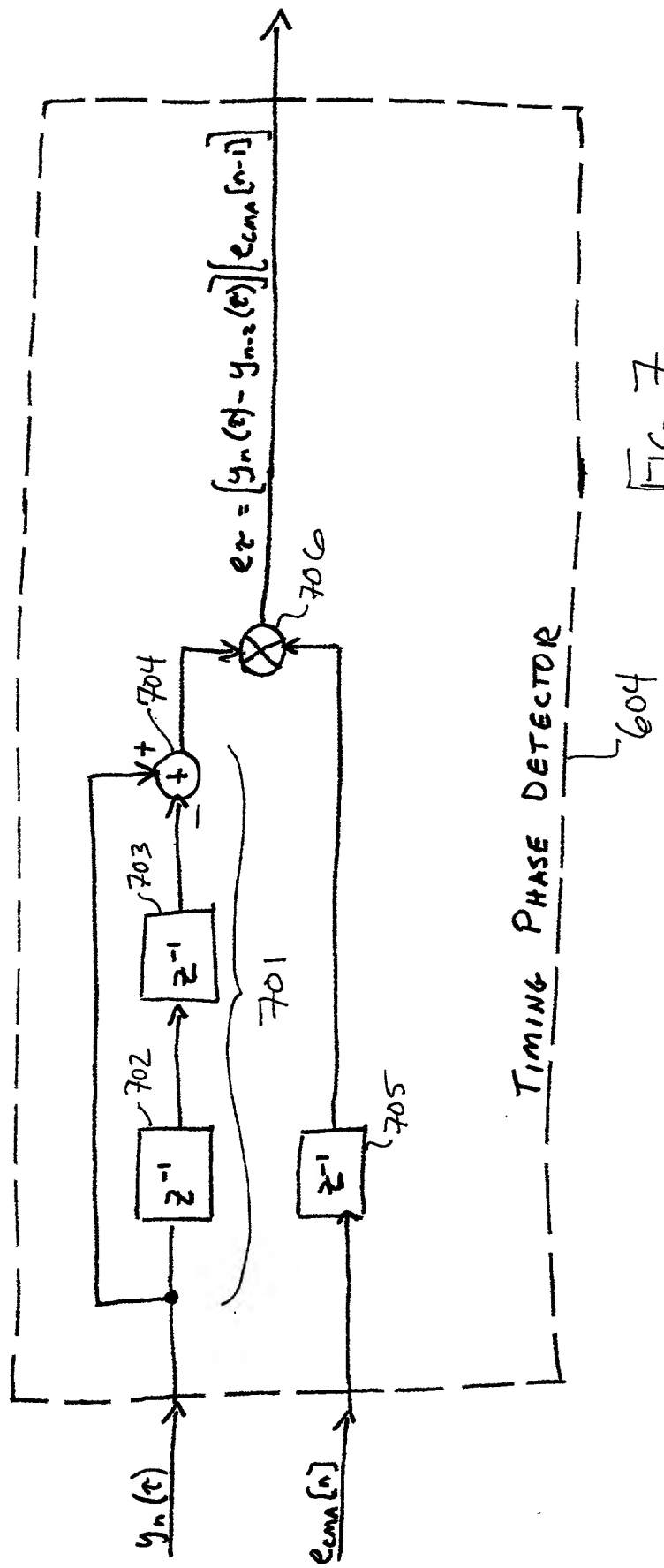


FIG. 7

FIG. 8 is a block diagram of a timing phase detector in accordance with the present invention. The timing phase detector 604 is shown in a dashed box. It receives an input signal  $y_n(t)$  and a reference signal  $SQM$ . The input signal  $y_n(t)$  is processed by a series of delay elements  $z^{-1}$  (802, 803) and a summer 804 to produce an error signal  $e_{ema}[n]$ . The reference signal  $SQM$  is processed by a series of delay elements  $z^{-1}$  (805, 806) and a summer 807 to produce an error signal  $e_{ema}[n]$ . The error signals  $e_{ema}[n]$  are then multiplied together in a multiplier 808 to produce the final output  $e_r$ .

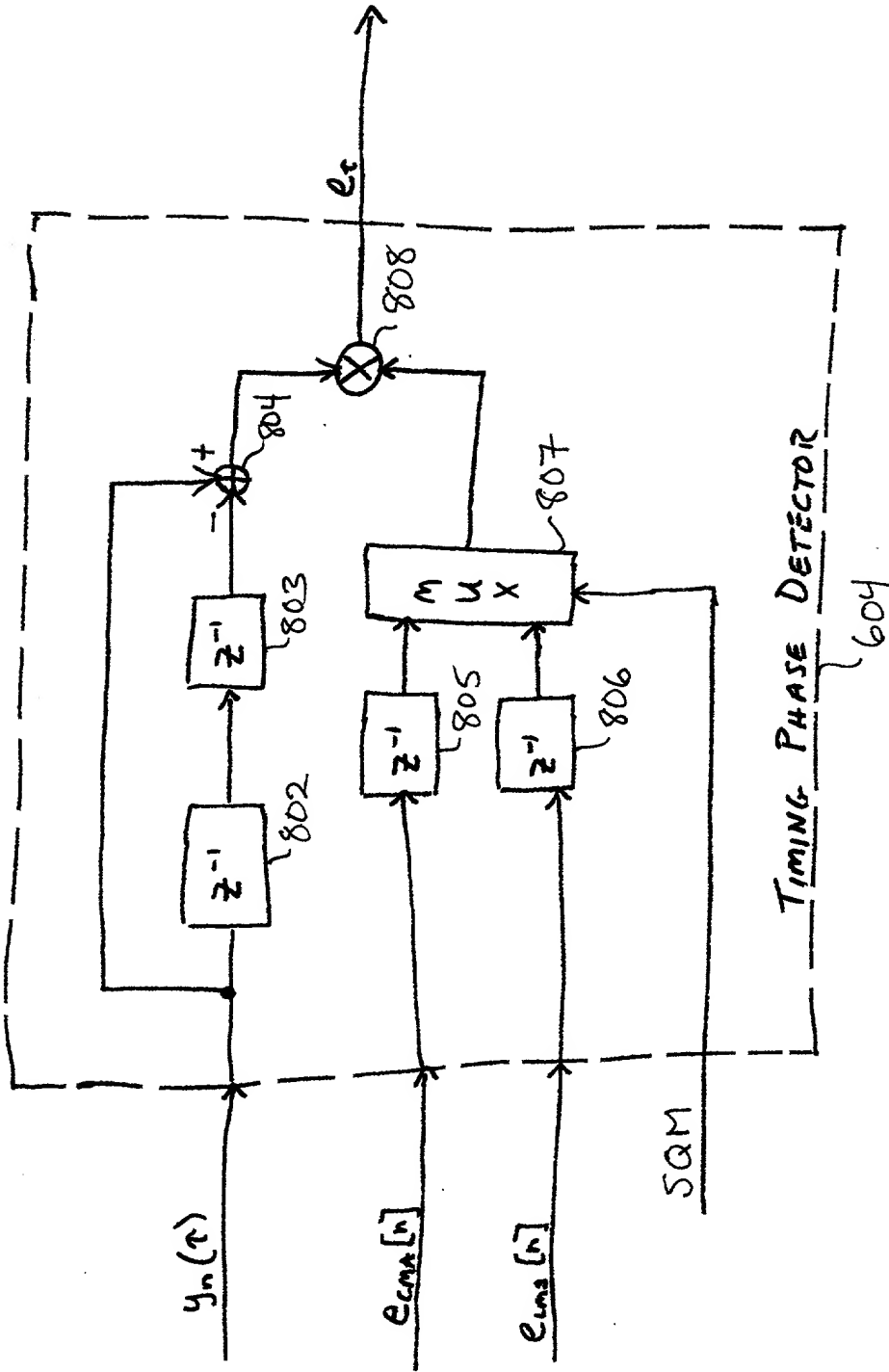
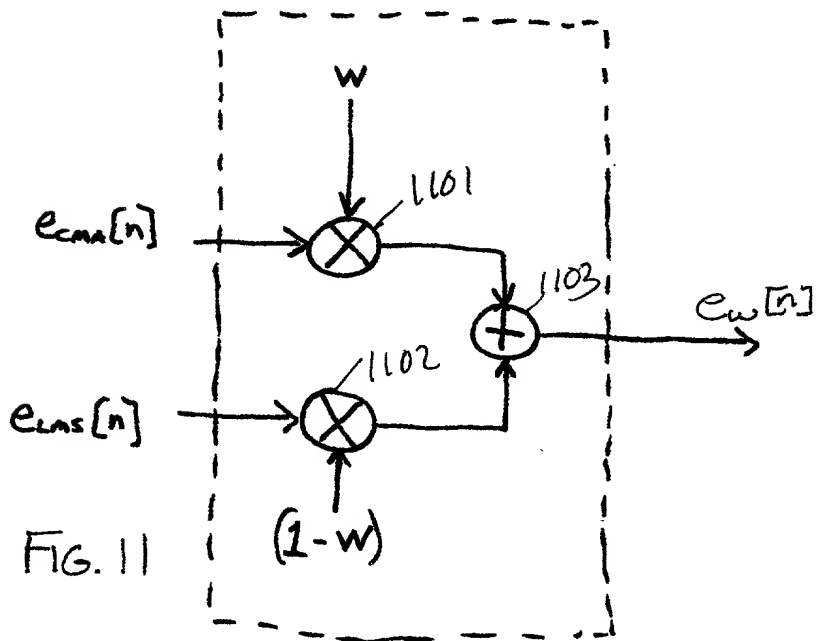
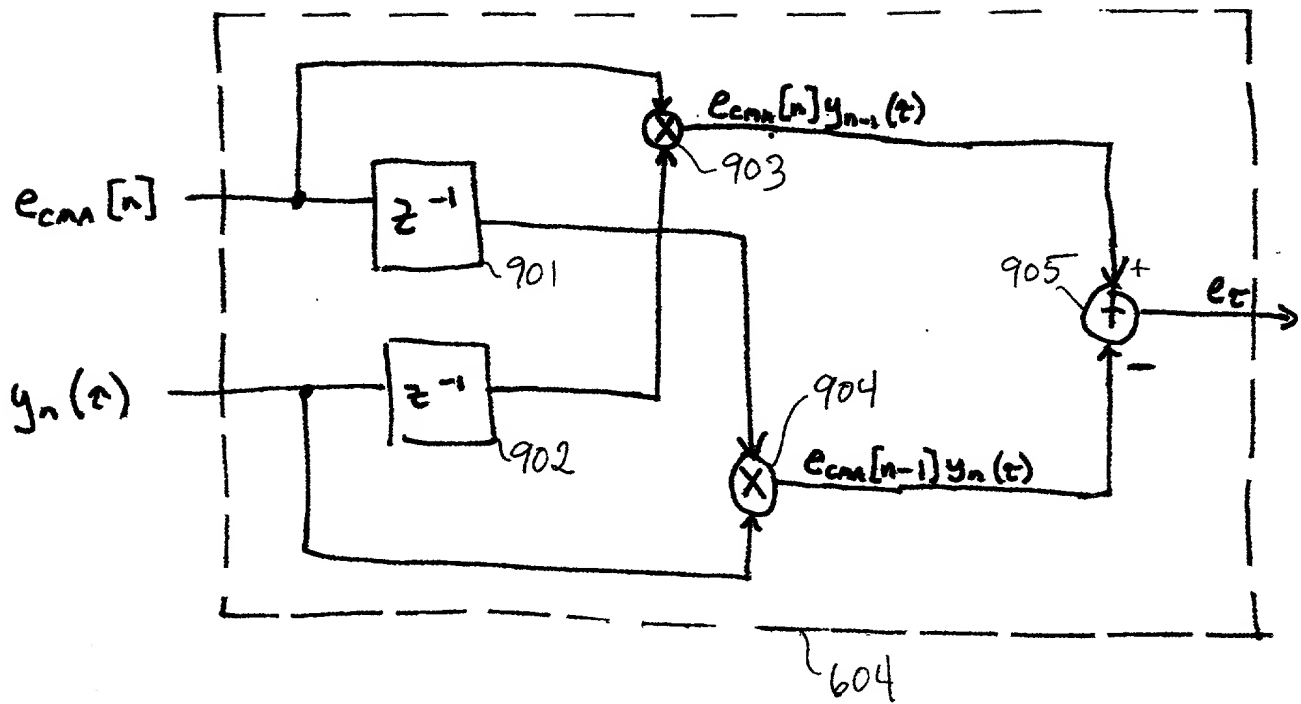


FIG. 8





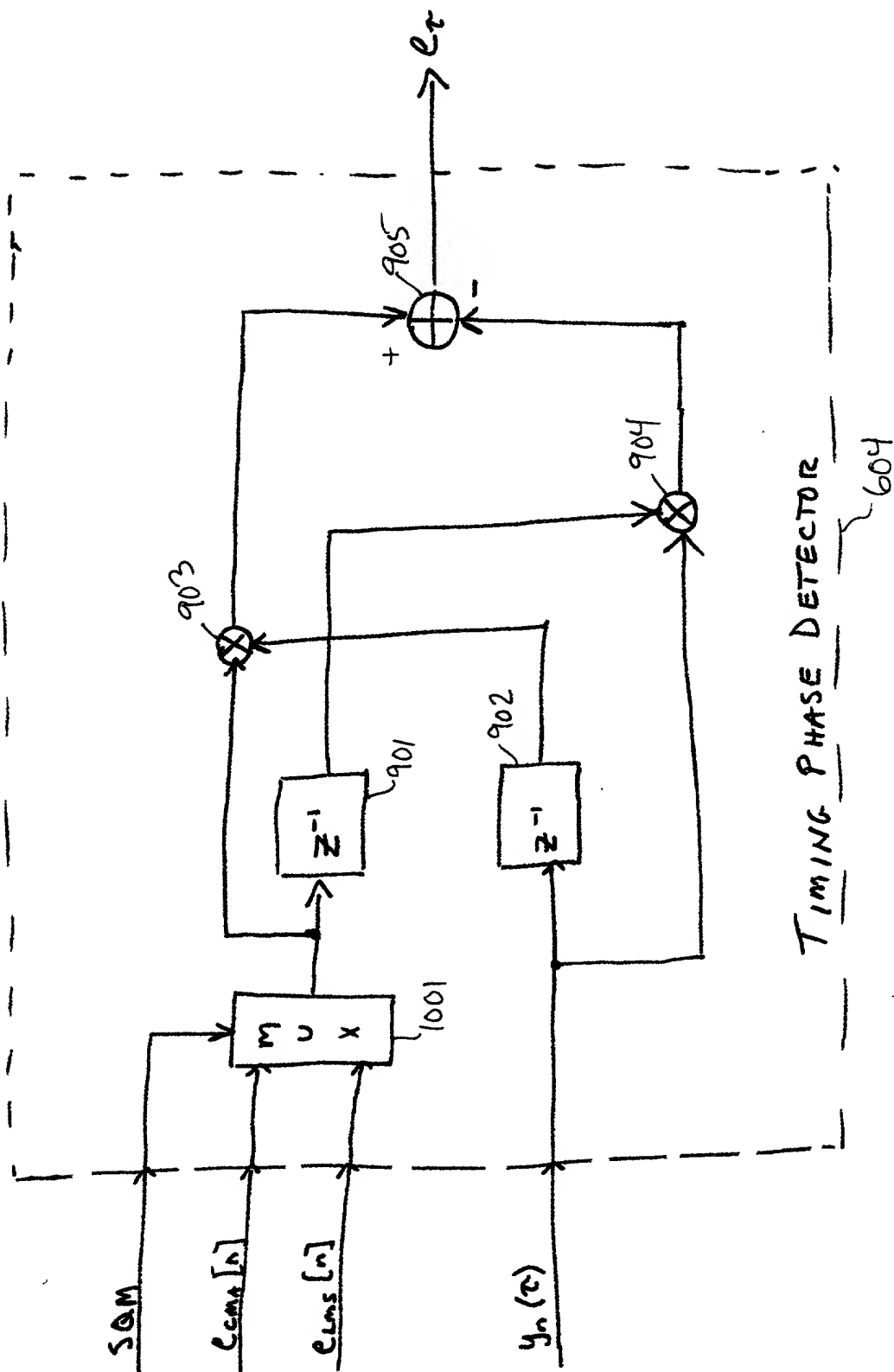


FIGURE 10

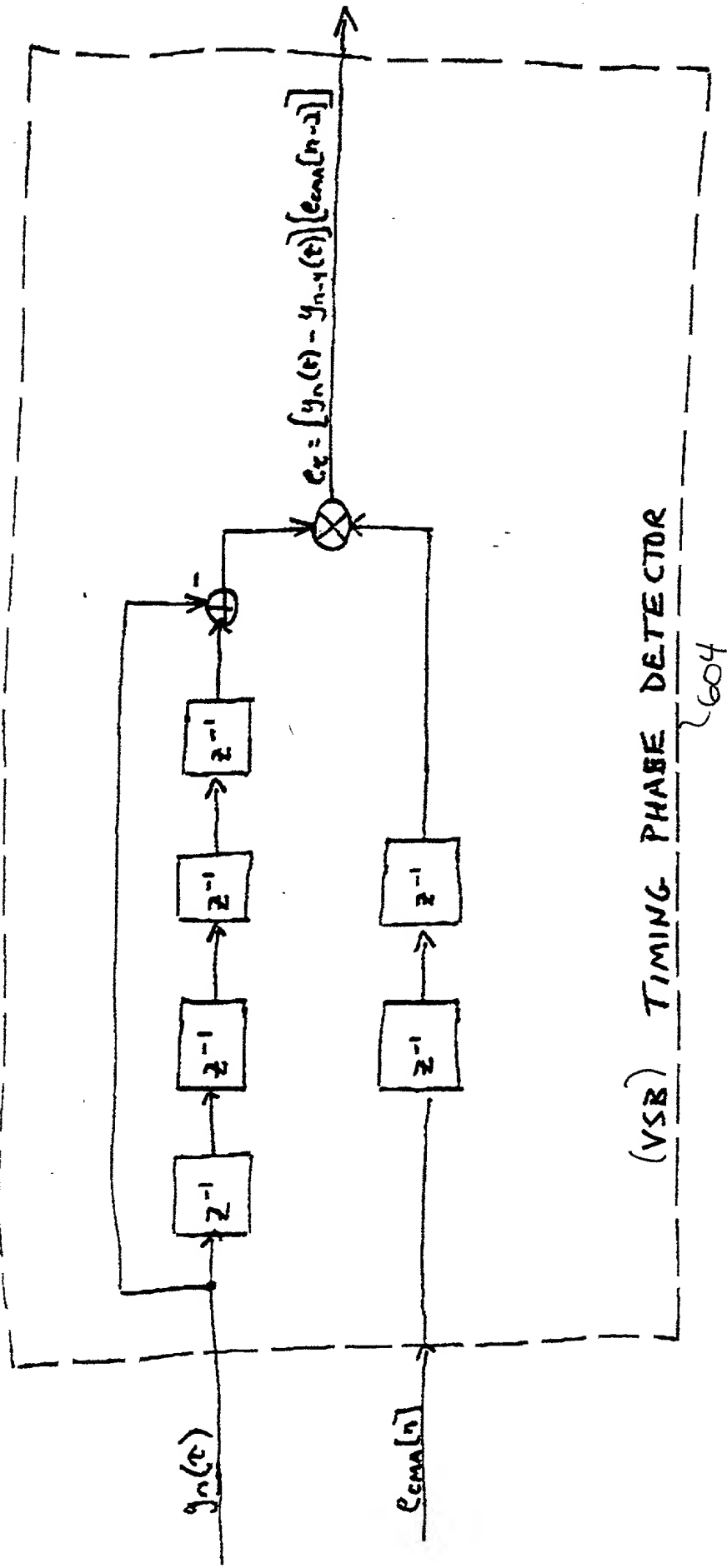


FIGURE 12

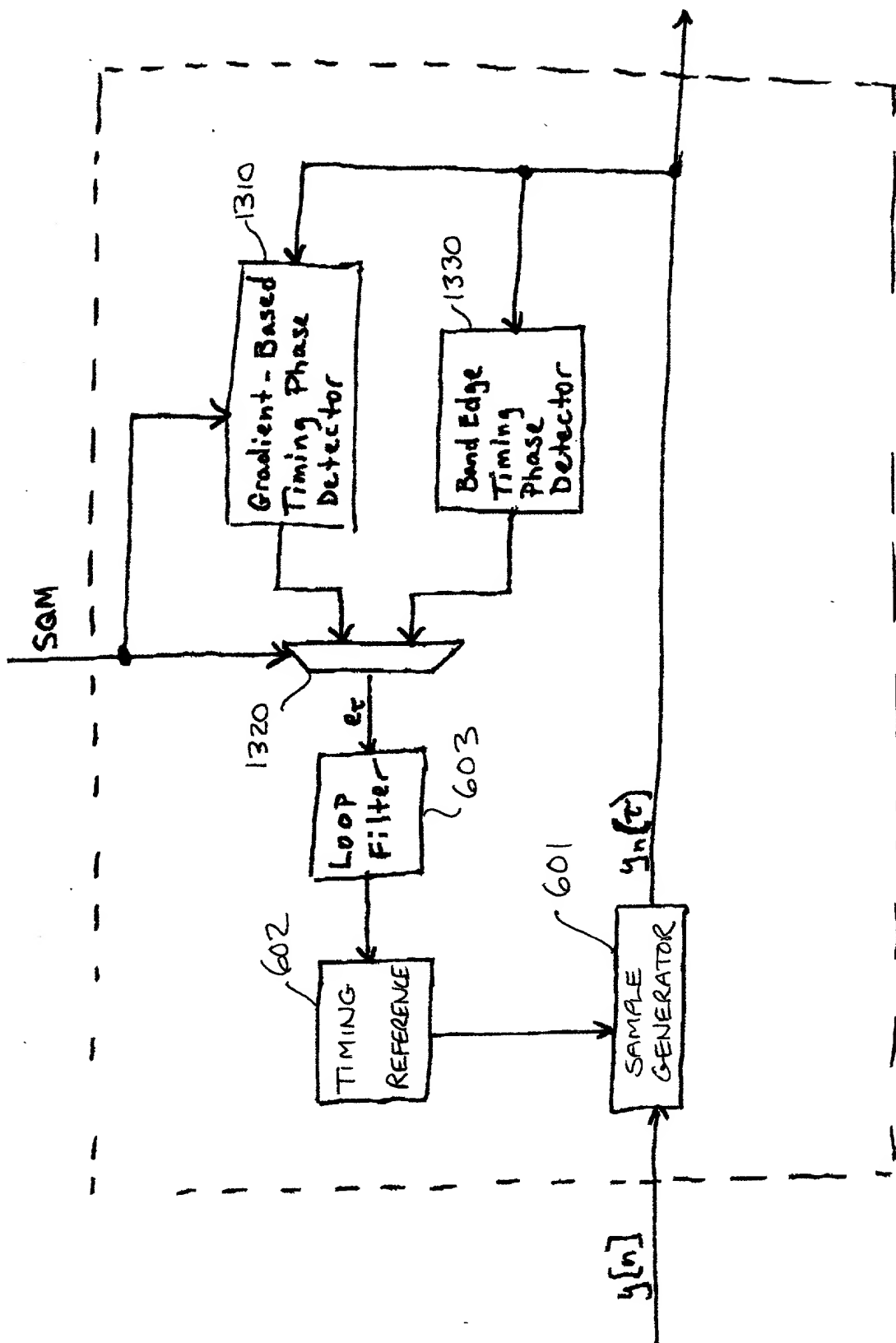


FIG. 13